(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 February 2004 (12.02.2004)

PCT

(10) International Publication Number
WO 2004/013971 A1

(51) International Patent Classification[7]: H03M 1/54

(21) International Application Number:
PCT/EP2003/008642

(22) International Filing Date: 31 July 2003 (31.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/400,178 31 July 2002 (31.07.2002) US

(71) Applicants and
(72) Inventors: AUGUSTO, Carlos, J., R., P. [PT/US]; 2233 Gunar Drive, San Jose, CA 95124 (US). DINIZ, Pedro, N., C. [PT/US]; 18709 San Gabriel Avenue, Cerritos, CA 90703 (US).

(74) Agent: VANDERPERRE, Robert; 6/8, Avenue de la Charmille, B-1200 Bruxelles (BE).

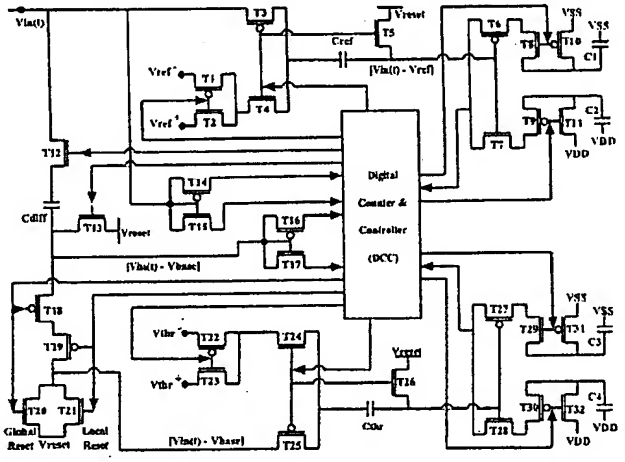
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ASYNCHRONOUS SERIAL ANALOG-TO-DIGITAL CONVERTER METHODOLOGY HAVING DYNAMIC ADJUSTMENT OF THE BANDWITH



(57) Abstract: A new methodology is disclosed to convert analog electric signals into digital data. The method provides a serial scheme without pre-definition of the number of bits (dynamic range). It allows digital processing of the input signal without sampling and holding of the input signal. Processing of the input signal is clock-less and asynchronously dependent on the time-evolution of the input signal itself. Thereby, a programmable, dynamic adjustment of bandwidth (product of dynamic range and speed of conversion) of the analog-to-digital conversion process can be achieved depending on the characteristics of the input signal. Dynamic adjustment of the bandwidth is accomplished by digitally controlling a "threshold" value at the input capacitor of the comparator, which when met by the input signal, triggers a transition at the output of the comparator.

WO 2004/013971 A1